3D-Integrated CMOS-NEMS Circuits for Energy Efficient Electronics

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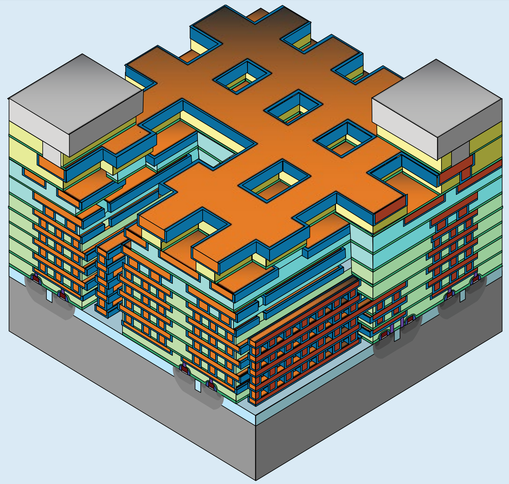
Motivation

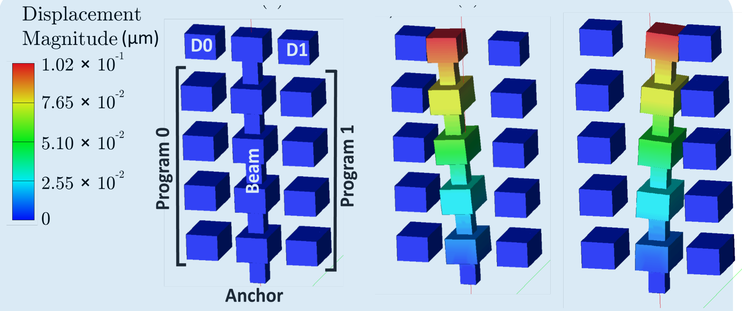
Internet of Things (IoT) necessitates the proliferation of edge computing devices requiring high energy efficiency. BEOL implementation of hybrid CMOS-NEMS circuits can achieve orders of magnitude greater energy efficiency than pure CMOS implementation.



Possible applications:

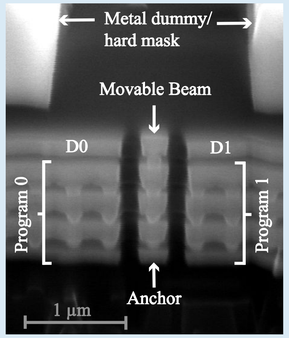
- Reconfigurable fast look-up table
- Fast data searching operation
- Compact energy efficient FPGA
- Power gating

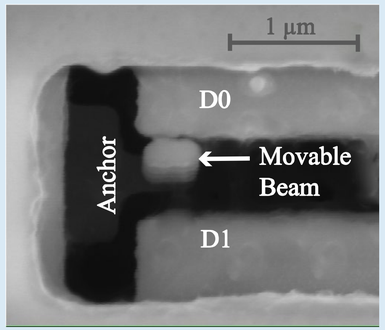
Monolithic Integration Approach



- **Nanometer CMOS processes have small (<30 nm) metal pitch**

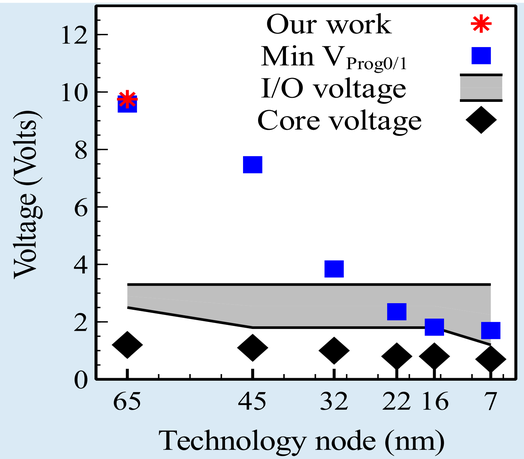
  → **Suited for implementation of compact NEM switches**





- **Non-volatile**
- **Low contact resistance (~kΩ) → small RC delay**

Performance Benchmarking



- **Program voltages become CMOS-compatible at advanced nodes**

Performance Parameter	Vertical NEM (5nm node)	SRAM
Bit cell size	~ 46 F^2	>100 F^2
Write energy	~ 20 aJ	< 100 fJ
Write delay	11.8 ns	< 50ps
Read energy	< 1 pJ	< 1 pJ
Read delay	<1 ns	< 50 ps

- **At 5 nm node:**
  - **Bitcell footprint < SRAM footprint**
  - **Write energy ≪ SRAM write energy**

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