Materials, Device, and Array Design for Next-Generation Ferroelectric Memory Technologies

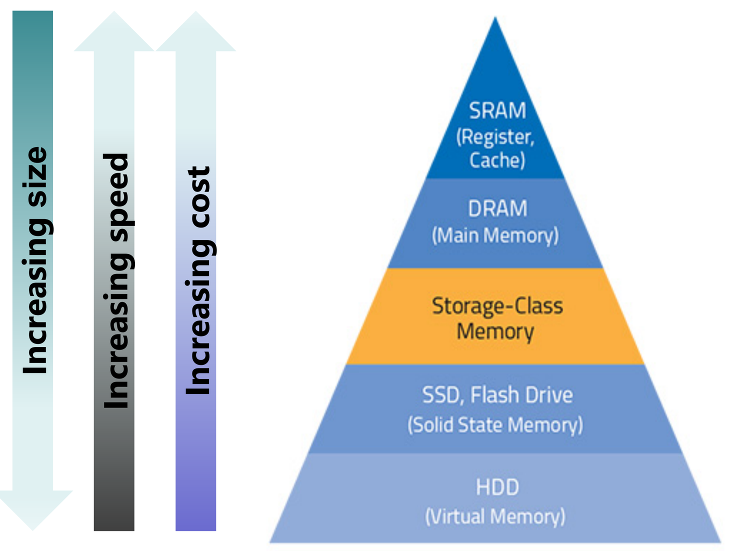
Ava J. Tan

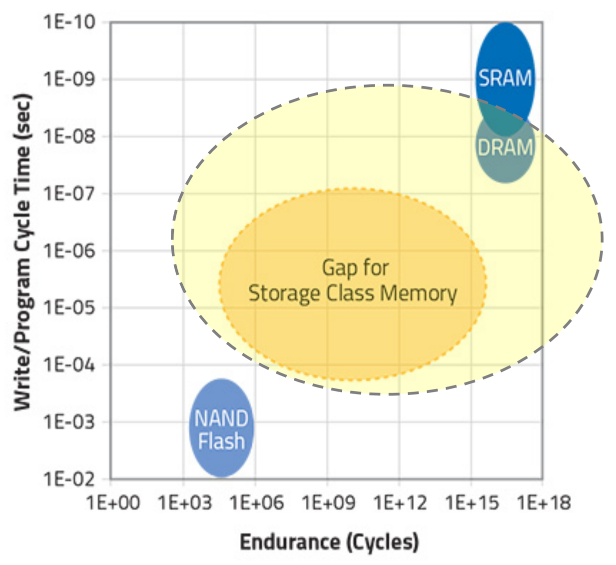
Department of Electrical Engineering & Computer Sciences, University of California Berkeley, Berkeley, CA, USA

I. OVERVIEW

In this work, I will present the ground-up development of ferroelectric CMOS-compatible oxides (doped hafnium oxide, or HfO2), device design based on these ferroelectric oxides (from ferroelectric capacitors to FeFETs, or ferroelectric transistors), to an experimental demonstration of a content addressable memory (CAM) cell based on FeFETs. I will discuss the various engineering challenges associated with developing a CMOS-compatible ferroelectric oxide for memory applications, device-specific performance challenges (endurance, reliability, etc.), and steps taken to mitigate some of these bottlenecks. The end goal is to develop a nonvolatile memory element that can be used for embedded memory applications or for in-memory computing. The properties of doped HfO2-based FeFETs in terms of fast write/read speeds, low voltage requirements, and retention robustness make them well-suited to accommodate modern computational needs by sealing the gaps between conventional memory, logic, and continued device scaling.

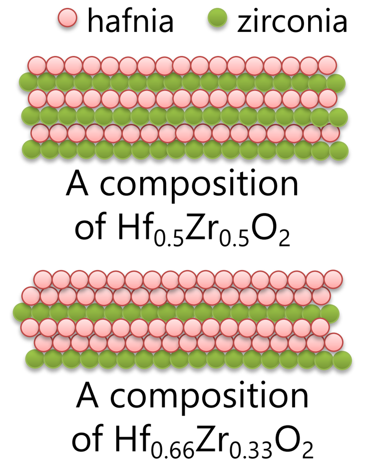
II. INTRO: The Market for Memory





- Mature technology exists for solid state memory and main memory, respectively
- Increasing performance requirements dictate need for innovation in **storage-class memory**

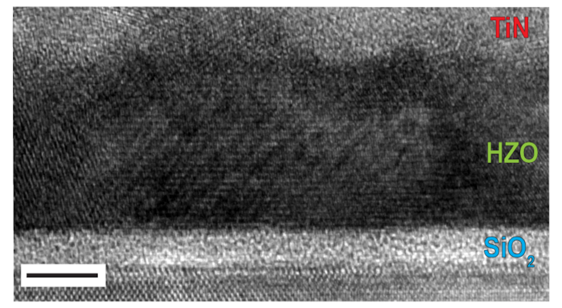
III. A) MATERIALS: Growth of Doped FE-HFO_2



A composition of $Hf_{0.5}Zr_{0.5}O_2$

A composition of $Hf_{0.66}Zr_{0.33}O_2$

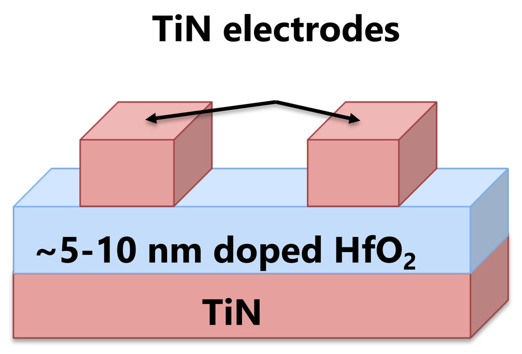
Subject film to RTA with a metal cap



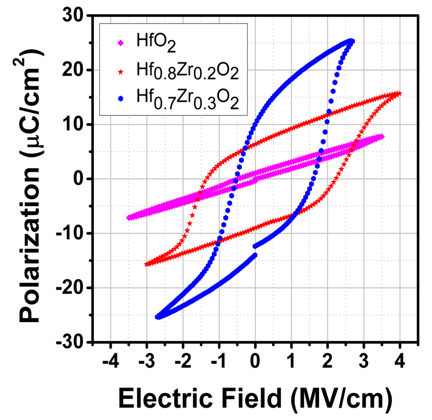
TEM image of a TiN-capped hafnium-zirconium oxide (HZO) sample after RTA.

- Dopant layering + confinement with metal cap + annealing = ferroelectric HfO_2!
- Other common dopants: **Si** (tested), **Al** (tested), Sr, Gd, Y, La ...
- **Key is to invoke strain in the film / induce o-vacancy formation**

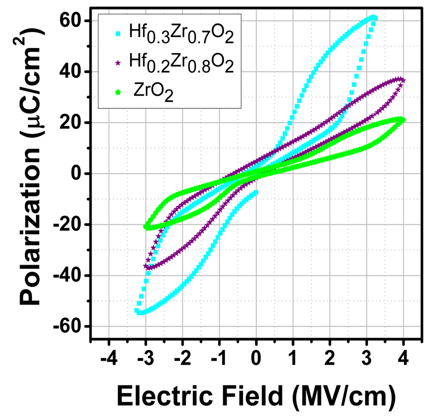
III. B) MATERIALS: Characterization of Doped HfO_2



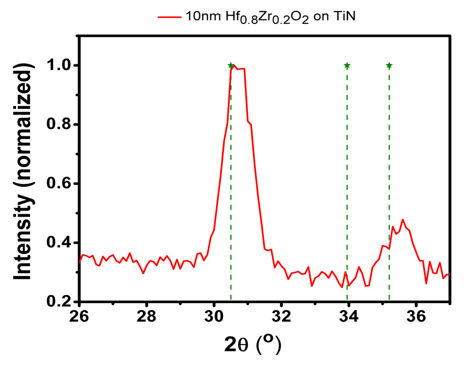
Simple MIM (metal-insulator-metal) device structure realized with only one lithography step to characterize doped HfO2 films.



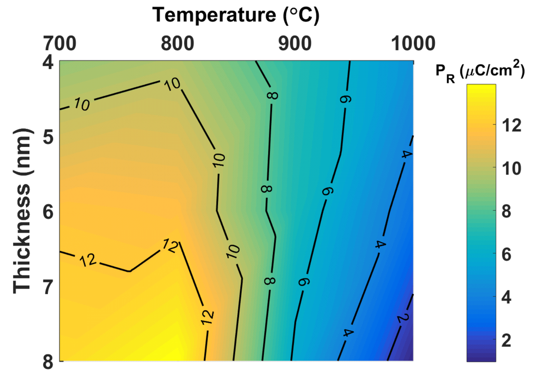
Hafnium-rich (x > 0.5) *films tend to be ferroelectric in nature.*



Zirconium-rich (x < 0.5) *films tend to be antiferroelectric in nature.*



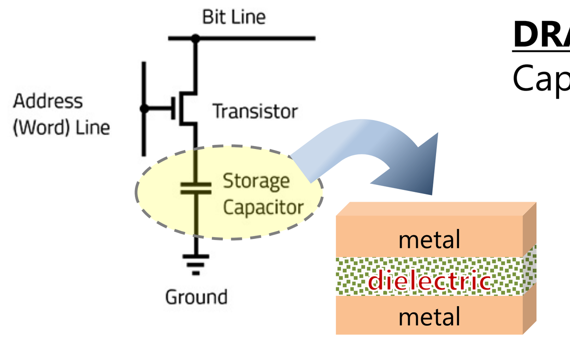
GIXRD is often used as an additional check for ferroelectricity/anti-ferroelectricity, indicated by the orthorhombic/tetragonal crystalline phases, respectively.



2D contour plot of remanent polarization vs. annealing temperature and film thickness.

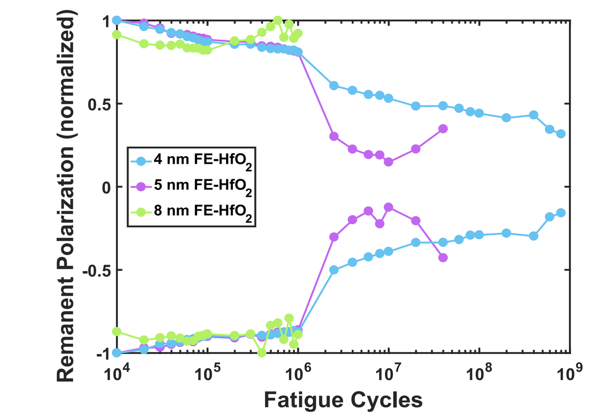
- G. Karbasian, **A. Tan** et al., 2017 *IEEE VLSI-TSA, Hsinchu, Taiwan. 2017.*
- **A. J. Tan** et al., 2019 *IEEE VLSI-TSA, Hsinchu, Taiwan. 2019.*

IV. A) DEVICES: FeRAM Characterization

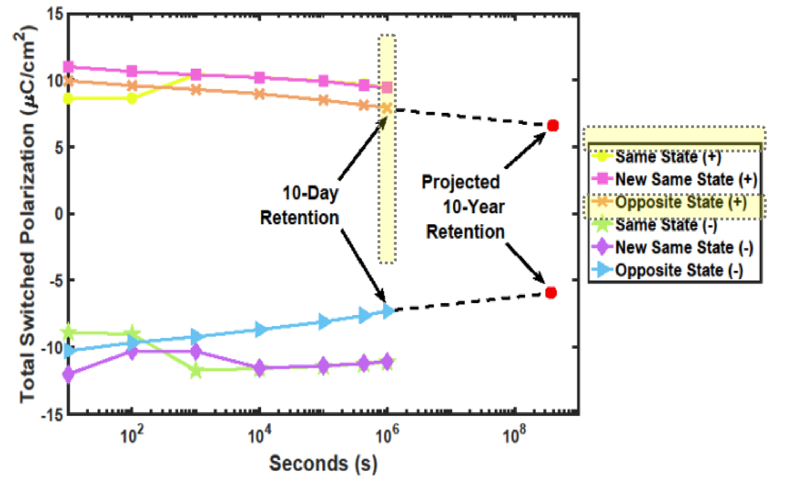


DRAM Key Trend: Constant Scaling for Increased Capacity

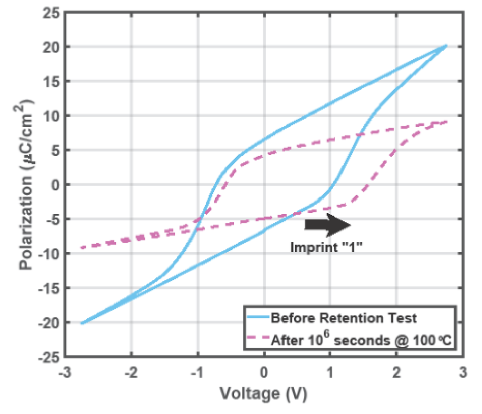
1. higher refresh rates → compromises energy efficiency
2. read circuitry needs improved charge sensitivity
3. higher aspect ratio etches and dielectric constants

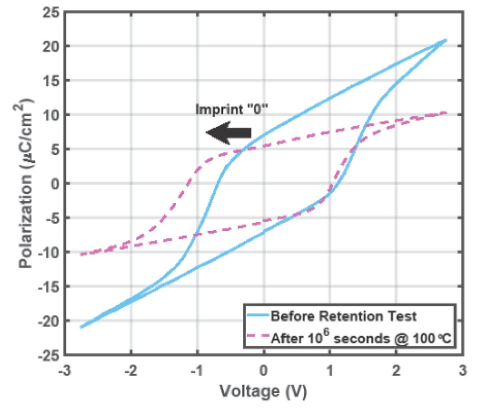


Endurance cycles till failure for 4, 5, and 8 nm FE-HfO₂ films (cycled at the same equivalent field of 2.5 MV/cm)



Retention testing for a typical 8 nm ferroelectric film at 100 °C.

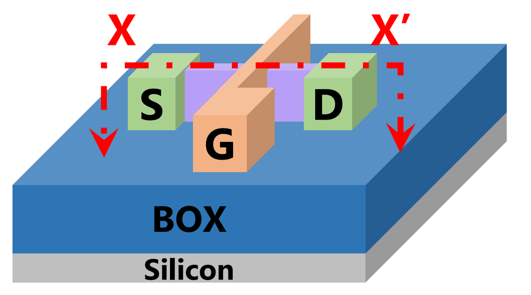




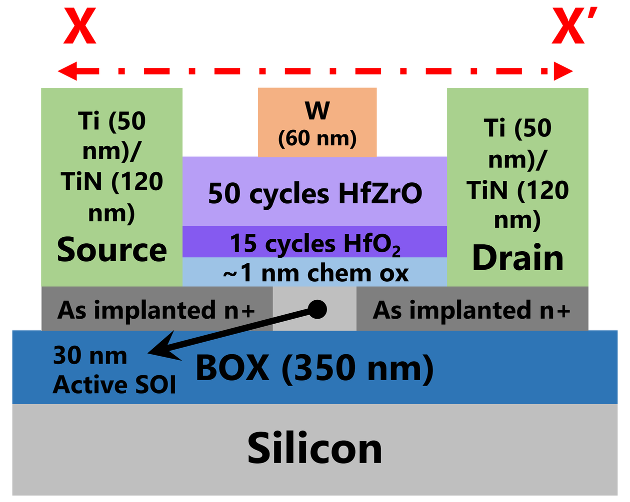
Imprint behavior is evaluated ***after ~ 1 month*** *at elevated temperature retention testing. Noticeable left/right shift of hysteresis loop indication of imprinting.*

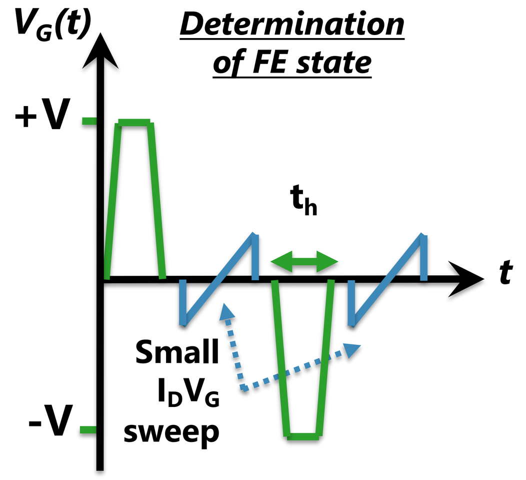
A. J. Tan *et al., 2019 IEEE VLSI-TSA, Hsinchu, Taiwan. 2019.*

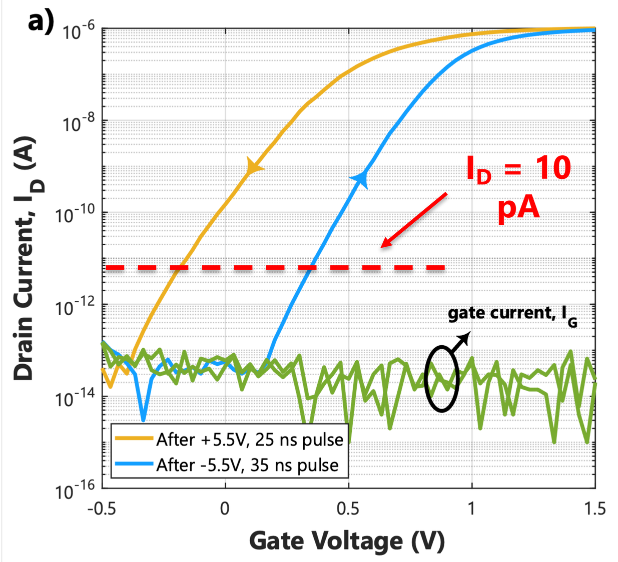
IV. B) DEVICES: FeFET Fabrication/Characterization



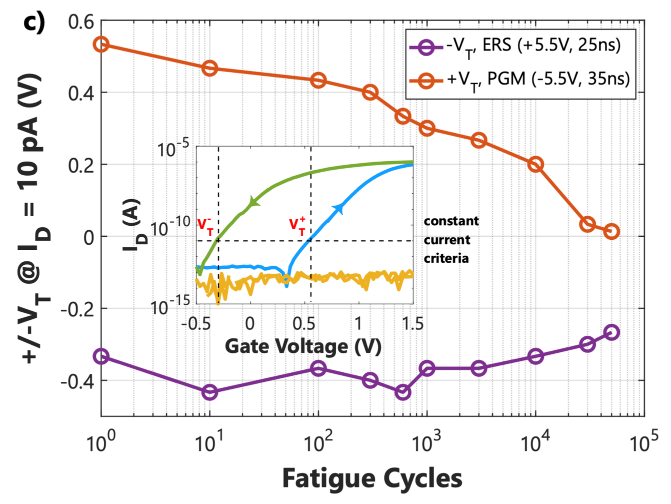
Fabricated via a gate-first, self-aligned process in Berkeley Marvell Nanofabrication Facility



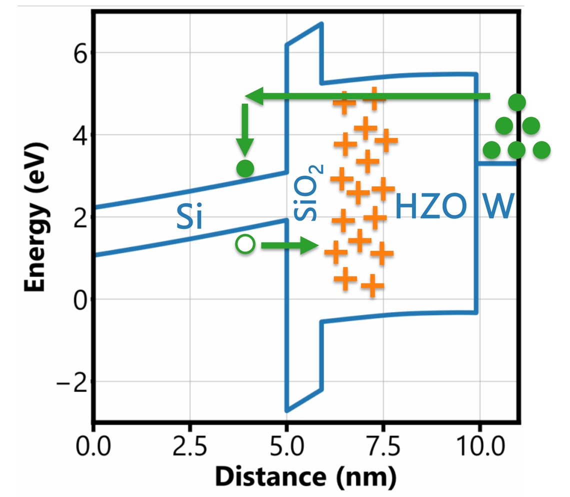




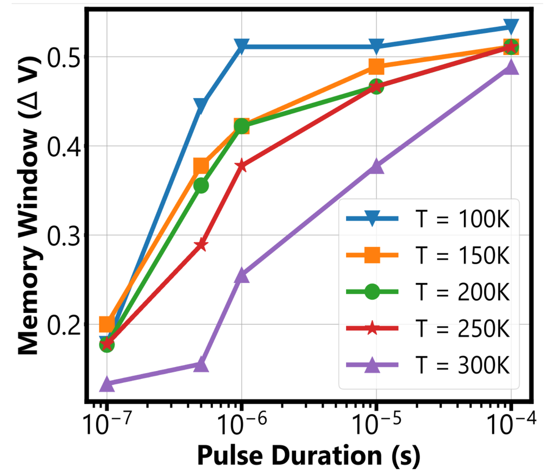
Left: *how state determination is electrically measured for a single FeFET.*
Right: *Resulting IDVG, with dashed red line marking two threshold voltages.*



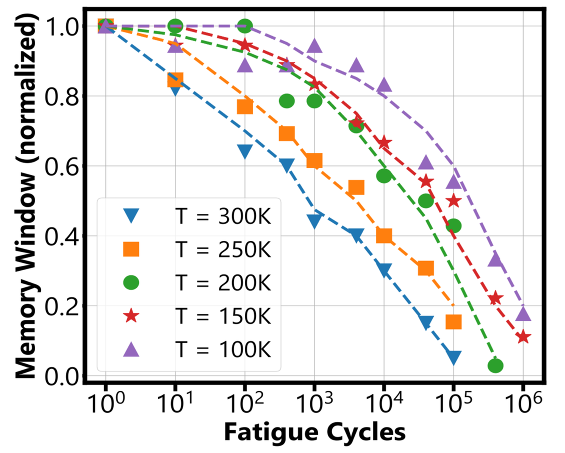
Typical endurance characteristics of an FeFET. PGM, ERS, and cycling conditions are +/-5.5V, 25 ns/35 ns.



Proposed FE degradation mechanism by hot electrons (confirmed with T-dependent studies below).



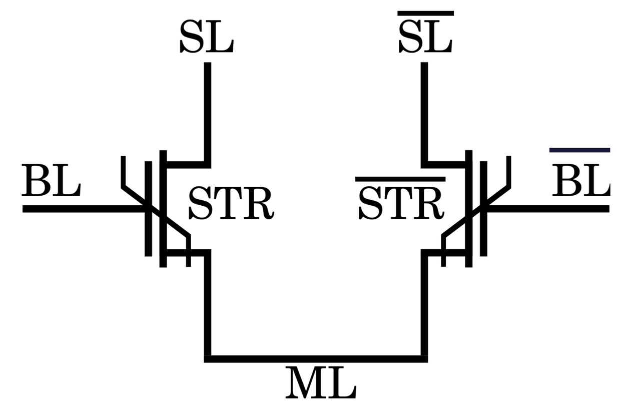
MW vs. program/erase pulse duration as a function of temperature. Voltages fixed at +/- 3.3V.



The % decrease in MW drops as measurement temperature decreases, allowing for the MW to persist for longer.

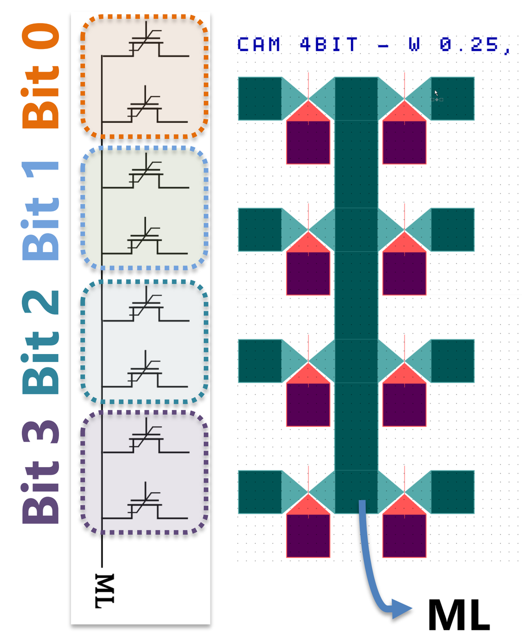
- **A. J. Tan** et al., 2020 IEEE EDL, 41(2), pp. 240-243, 2020.
- **A. J. Tan** et al., 2020 IEEE VLSI, Honolulu, HI, USA. 2020.
- **A. J. Tan** et al., 2020 DRC, Columbus, OH, USA,. 2020.

V) ARRAY: FeCAM Design and Testing

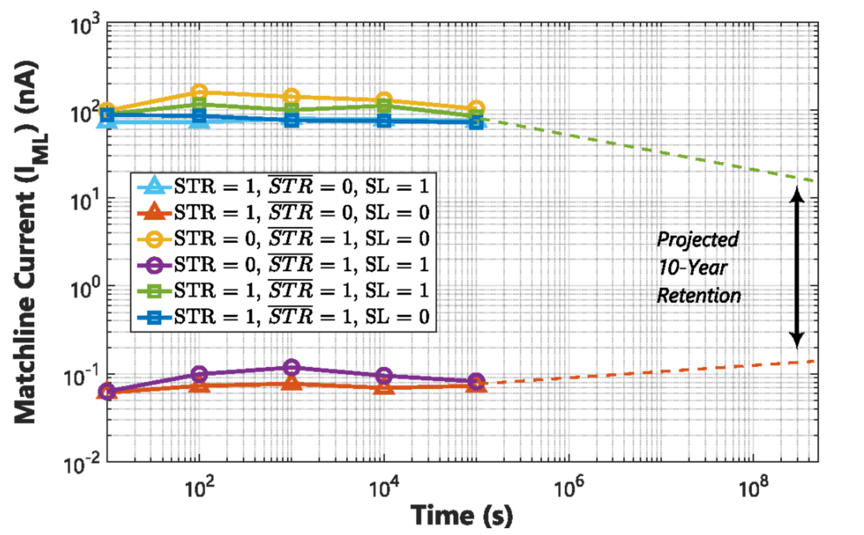


SL (V_D)	STR (V_{PGM})	ML (I_D)
0 V	-5 V	10.9 nA
0 V	+5 V	3.21 pA
50 mV	-5 V	2.79 pA
50 mV	+5 V	13.1 nA

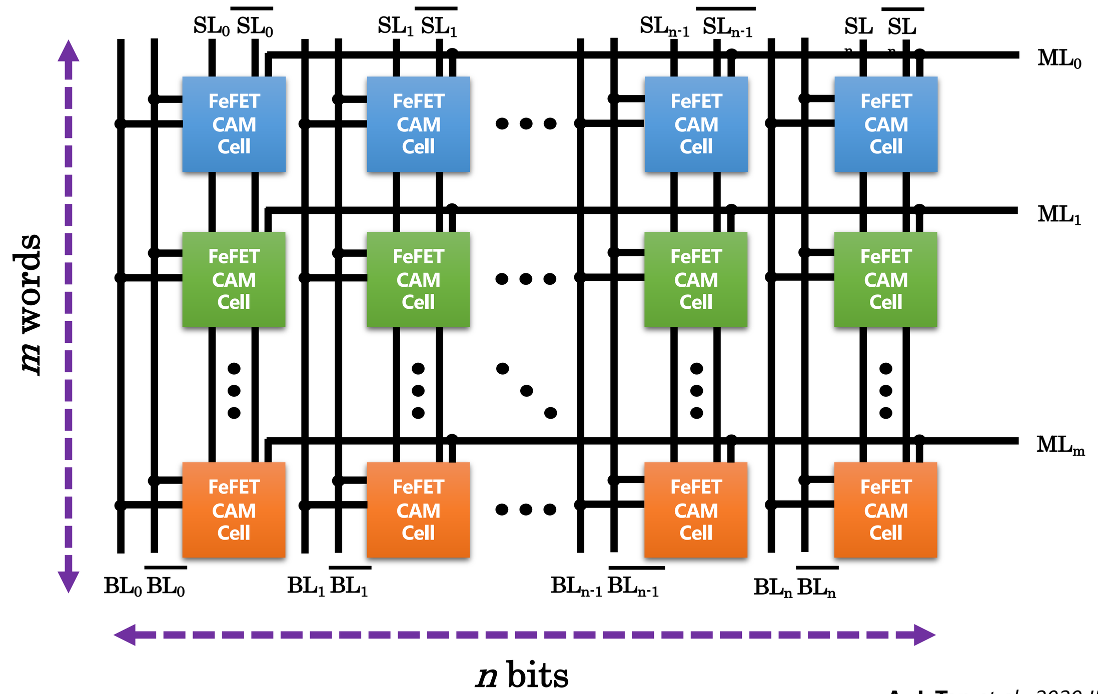
- **Two-FeFET CAM cell for XNOR function implementation:** A bit and its complement are written to *STR* and $\overline{STR}$, respectively
- During search – search bit and complement broadcasted on *SL* and $\overline{SL}$, gates of FeFETs grounded
- Current on ML is read on each bit and summed with ML current contributions from all other bits in word ***(table shows sample ML readout current from one cell)***



4-bit CAM word layout (testing currently in progress)



Retention testing for all 6 state possibilities of the XNOR function for the 2-FeFET CAM cell. Two additional cases for forced matches are also tested.



Proposed m x n FECAM array, to be fabricated and tested in future works. Each individual CAM cell is a 2-FeFET cell as described above. This FECAM array is projected to allow for rapid lookup and identification of existing data in memory, which is advantageous for brain-inspired computing.

A. J. Tan et al., 2020 IEEE EDL, 41(2), pp. 240-243, 2020.

VI) Acknowledgements

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